CLAIMS

1-29. (Canceled)

30. (New) An interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network, the interface circuit comprising:

(a) filter circuitry configured to separate low-frequency and high-frequency signals appearing on the tip/ring lines, wherein the filter circuitry comprises a blocking capacitor that affects the impedance of the tip/ring lines;

(b) high-frequency interface circuitry configured to process the high-frequency signals;

(c) low-frequency interface circuitry configured to process the low-frequency signals, wherein the low-frequency interface circuitry comprises:

(1) a subscriber line interface circuit (SLIC) configured between the tip and ring lines; and

(2) a coder/decoder (CODEC) coupled to the SLIC and configured to encode and decode the low-frequency signals;

(d) a capacitor cancellation circuit (CCC) coupled across the blocking capacitor and adapted to generate a first single-ended signal, which is applied to the SLIC and coupled via the SLIC and the filter circuitry to the tip/ring lines to cancel a portion of the effect of the blocking capacitor on the impedance of the tip/ring lines.

31. (New) The invention of claim 30, wherein the cancellation provided by the CCC provides a desired impedance between the tip/ring lines for both the low-frequency and high-frequency signals.

32. (New) The invention of claim 31, wherein the desired impedance has a resistance of about 900 ohms and a capacitance of about 2.16 microfarads.

33. (New) The invention of claim 30, wherein the portion canceled by the CCC corresponds to at least about 90% of the effect induced by the blocking capacitor.

34. (New) The invention of claim 30, wherein the CCC comprises:

a first converter adapted to sense a differential voltage across the blocking capacitor and generate a single-ended capacitance signal that reflects the capacitance of the blocking capacitor; and

a low-pass filter adapted to filter out components of the single-ended capacitance signal corresponding to the high-frequency signals to generate the first single-ended signal.

35. (New) The invention of claim 34, wherein the CODEC is coupled to the SLIC via a second converter adapted to convert a pair of differential signals generated by the CODEC into a second single-ended signal applied to the SLIC.

36. (New) The invention of claim 34, wherein the first converter comprises an operational amplifier having two inputs coupled across the blocking capacitor and an output coupled to the low-pass filter.

37. (New) The invention of claim 36, wherein the first converter comprises:

a first capacitor and a first resistor coupled in series between a non-inverting input of the operational amplifier and a first terminal of the blocking capacitor;

a second capacitor and a second resistor coupled in series between an inverting input of the operational amplifier and a first terminal of the blocking capacitor;

a third capacitor and a third resistor coupled in parallel between the inverting input and the output of the operational amplifier; and

a fourth capacitor and a fourth resistor coupled in parallel between the non-inverting input of the operational amplifier and the SLIC.

38. (New) The invention of claim 34, wherein the low-pass filter is a fourth-order filter.

39. (New) The invention of claim 38, wherein the low-pass filter comprises two serially connected second-order filters.

40. (New) The invention of claim 30, wherein:

the high-frequency signals correspond to DSL signals having frequencies greater than about 4 kHz;

the low-frequency signals correspond to POTS signals having frequencies less than about 4 kHz; and

the filter circuitry comprises (i) a high-pass filter configured to provide the DSL signals to the high-frequency interface circuitry and (ii) a low-pass filter configured to provide the POTS signals to the low-frequency interface circuitry, wherein the blocking capacitor is part of the high-pass filter.

41. (New) A capacitor cancellation circuit (CCC) for an interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network, the interface circuit comprising:

(a) filter circuitry configured to separate low-frequency and high-frequency signals appearing on the tip/ring lines, wherein the filter circuitry comprises a blocking capacitor that affects the impedance of the tip/ring lines;

(b) high-frequency interface circuitry configured to process the high-frequency signals;

(c) low-frequency interface circuitry configured to process the low-frequency signals, wherein the low-frequency interface circuitry comprises:

(1) a subscriber line interface circuit (SLIC) configured between the tip and ring lines; and

(2) a coder/decoder (CODEC) coupled to the SLIC and configured to encode and decode the low-frequency signals;

(d) the capacitor cancellation circuit (CCC) coupled across the blocking capacitor and adapted to generate a first single-ended signal, which is applied to the SLIC and coupled via the SLIC and the filter circuitry to the tip/ring lines to cancel a portion of the effect of the blocking capacitor on the impedance of the tip/ring lines.

42. (New) The invention of claim 41, wherein the cancellation provided by the CCC provides a desired impedance between the tip/ring lines for both the low-frequency and high-frequency signals.

43. (New) The invention of claim 41, wherein the portion canceled by the CCC corresponds to at least about 90% of the effect induced by the blocking capacitor.

44. (New) The invention of claim 41, wherein the CCC comprises:

a first converter adapted to sense a differential voltage across the blocking capacitor and generate a single-ended capacitance signal that reflects the capacitance of the blocking capacitor; and

a low-pass filter adapted to filter out components of the single-ended capacitance signal corresponding to the high-frequency signals to generate the first single-ended signal.

45. (New) The invention of claim 44, wherein the CODEC is coupled to the SLIC via a second converter adapted to convert a pair of differential signals generated by the CODEC into a second single-ended signal applied to the SLIC.

46. (New) The invention of claim 44, wherein the first converter comprises an operational amplifier having two inputs coupled across the blocking capacitor and an output coupled to the low-pass filter.

47. (New) The invention of claim 46, wherein the first converter comprises:

a first capacitor and a first resistor coupled in series between a non-inverting input of the operational amplifier and a first terminal of the blocking capacitor;

a second capacitor and a second resistor coupled in series between an inverting input of the operational amplifier and a first terminal of the blocking capacitor;

a third capacitor and a third resistor coupled in parallel between the inverting input and the output of the operational amplifier; and

a fourth capacitor and a fourth resistor coupled in parallel between the non-inverting input of the operational amplifier and the SLIC.

48. (New) The invention of claim 44, wherein the low-pass filter is a fourth-order filter.

49. (New) The invention of claim 48, wherein the low-pass filter comprises two serially connected second-order filters.

50. (New) An interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network, the interface circuit comprising:

(a) filter circuitry configured to separate low-frequency and high-frequency signals appearing on the tip/ring lines, wherein the filter circuitry comprises a blocking capacitor that affects the impedance of the tip/ring lines;

(b) high-frequency interface circuitry configured to process the high-frequency signals;

(c) low-frequency interface circuitry configured to process the low-frequency signals, wherein the low-frequency interface circuitry comprises:

(1) a subscriber line interface circuit (SLIC) configured between the tip and ring lines; and

(2) a coder/decoder (CODEC) coupled to the SLIC and configured to encode and decode the low-frequency signals;

(d) a capacitor cancellation circuit (CCC) coupled across the blocking capacitor and adapted to cancel a portion of the effect of the blocking capacitor on the impedance of the tip/ring lines, wherein the CCC comprises:

an operational amplifier having (i) an inverting input coupled to a first terminal of the blocking capacitor, (ii) a non-inverting input coupled to a second terminal of the blocking capacitor, and (iii) an output coupled back to the first and second terminals of the blocking capacitor; and

an inverter coupled between the output of the operational amplifier and the first terminal of the blocking capacitor.

51. (New) The invention of claim 50, wherein the CCC further comprises:

a first capacitor and a first resistor coupled in series between the inverting input of the operational amplifier and the first terminal of the blocking capacitor;

a second capacitor and a second resistor coupled in series between the non-inverting input of the operational amplifier and the second terminal of the blocking capacitor;

a third capacitor and a third resistor coupled in parallel between the inverting input and the output of the operational amplifier; and

a fourth capacitor and a fourth resistor coupled in parallel between the non-inverting input of the operational amplifier and a ground terminal.

52. (New) The invention of claim 51, wherein the CCC further comprises:

a fifth capacitor and a fifth resistor coupled in series between the output of the operational amplifier and the second terminal of the blocking capacitor; and

a sixth capacitor and a sixth resistor coupled in series between the inverter and the first terminal of the blocking capacitor.

53. (New) The invention of claim 50, wherein the cancellation provided by the CCC provides a desired impedance between the tip/ring lines for both the low-frequency and high-frequency signals.

54. (New) The invention of claim 53, wherein the desired impedance has a resistance of about 900 ohms and a capacitance of about 2.16 microfarads.

55. (New) The invention of claim 50, wherein the portion canceled by the CCC corresponds to at least about 90% of the effect induced by the blocking capacitor.

56. (New) The invention of claim 50, wherein:

the high-frequency signals correspond to DSL signals having frequencies greater than about 4 kHz;

the low-frequency signals correspond to POTS signals having frequencies less than about 4 kHz; and

the filter circuitry comprises (i) a high-pass filter configured to provide the DSL signals to the high-frequency interface circuitry and (ii) a low-pass filter configured to provide the POTS signals to the low-frequency interface circuitry, wherein the blocking capacitor is part of the high-pass filter.

57. (New) A capacitor cancellation circuit(CCC) for an interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network, the interface circuit comprising:

(a) filter circuitry configured to separate low-frequency and high-frequency signals appearing on the tip/ring lines, wherein the filter circuitry comprises a blocking capacitor that affects the impedance of the tip/ring lines;

(b) high-frequency interface circuitry configured to process the high-frequency signals;

(c) low-frequency interface circuitry configured to process the low-frequency signals, wherein the low-frequency interface circuitry comprises:

(1) a subscriber line interface circuit (SLIC) configured between the tip and ring lines; and

(2) a coder/decoder (CODEC) coupled to the SLIC and configured to encode and decode the low-frequency signals;

(d) the capacitor cancellation circuit (CCC) coupled across the blocking capacitor and adapted to cancel a portion of the effect of the blocking capacitor on the impedance of the tip/ring lines, wherein the CCC comprises:

an operational amplifier having (i) an inverting input coupled to a first terminal of the blocking capacitor, (ii) a non-inverting input coupled to a second terminal of the blocking capacitor, and (iii) an output coupled back to the first and second terminals of the blocking capacitor; and

an inverter coupled between the output of the operational amplifier and the first terminal of the blocking capacitor.

58. (New) The invention of claim 57, wherein the CCC further comprises:

a first capacitor and a first resistor coupled in series between the inverting input of the operational amplifier and the first terminal of the blocking capacitor;

a second capacitor and a second resistor coupled in series between the non-inverting input of the operational amplifier and the second terminal of the blocking capacitor;

a third capacitor and a third resistor coupled in parallel between the inverting input and the output of the operational amplifier; and

a fourth capacitor and a fourth resistor coupled in parallel between the non-inverting input of the operational amplifier and a ground terminal.